WHAT IS CLAIMED IS:

1. A method of fabricating an LDMOS transistor and a conventional CMOS transistor together on a substrate, the method comprising:

implanting, into a surface of a substrate, a first impurity region (1304) with a first volume and a first surface area, the first impurity region being of a first type;

implanting, into the surface of the substrate, a second impurity region (106,122);

forming a gate oxide (1306) for a gate of the LDMOS transistor between a source region and a drain region of the LDMOS transistor;

covering the gate oxide with a conductive material (1310);

implanting, into a source region of the LDMOS transistor, a third impurity region (1312) with a second volume and a second surface area in the first surface area of the first impurity region, the third impurity region being of an opposite second type relative to the first type, the third impurity region being self aligned with respect to the gate of the LDMOS transistor;

forming a gate oxide (118,134) for a gate of the conventional CMOS transistor between a source region and a drain region of the conventional CMOS transistor, the gate oxide of the conventional CMOS transistor being formed after implantation of the third impurity region;

covering the gate oxide of the conventional CMOS transistor with a conductive material (120,136);

implanting, into the source region of the LDMOS transistor, a fourth impurity region (1318) with a third volume and a third surface area and a fifth impurity region (1316) with a fourth volume and a fourth surface area in the second surface area of the second impurity region, the fourth impurity region being of the first type, the fifth impurity region being of the opposite second type;

implanting, into the drain region of the LDMOS transistor, a sixth impurity region (1320) with a fifth volume and a fifth surface area, the sixth impurity region being of the first type;

implanting, into a source region of the conventional CMOS transistor, a seventh impurity region (112,128), the seventh impurity region being in the second impurity region; and

implanting, into a drain region of the conventional CMOS transistor, an eighth impurity region (114,130), the eighth impurity region being in the second impurity region.

2. The method of claim 1, wherein the fourth and sixth impurity regions are implanted at a same time using a same mask.

3. The method of claim 1, wherein the fifth, seventh, and eighth impurity regions are implanted at a same time using a same mask.

4. The method of claim 1, wherein the fourth, fifth, sixth, seventh, and eighth impurity regions are ohmic contacts.

5. The method of claim 1, further comprising implanting, into the drain region of the LDMOS transistor, a ninth impurity region (1314) with an eighth volume and an eighth surface area in the first surface area of the first impurity region, the ninth impurity region being implanted with a spacing from the third impurity region, the ninth impurity region being of the first type.

6. The method of claim 5, wherein the ninth impurity region is self aligned to the gate of the LDMOS transistor and is implanted after forming the gate of the LDMOS transistor.

7. The method of claim 5, wherein the ninth impurity region is non-self aligned to the gate of the LDMOS transistor and is implanted prior to forming of the gate of the LDMOS transistor.

8. The method of claim 5, wherein the spacing of the third impurity region from the ninth impurity region is sized such that the ninth impurity region is spaced a distance (*d*) away from the gate of the LDMOS transistor as measured along a surface of the LDMOS transistor.

9. The method of claim 5, wherein the first impurity region and the ninth impurity region are implanted using a same mask.

10. The method of claim 5, wherein the implantation of the ninth impurity region is defined by a slit mask, the ninth impurity region forming multiple implants (1812) spaced apart relative to each other along a surface in the drain region of the LDMOS transistor.

11. The method of claim 1, wherein implanting the third impurity region includes implanting the third impurity region using a first implant (802) and a second implant (804).

12. The method of claim 11, wherein the first implant is a high energy implant.

13. The method of claim 11, wherein the first implant is a large angle tilt implant.

14. The method of claim 1, further comprising implanting, into the source region of the LDMOS transistor, a tenth impurity region (1704) with a ninth volume having a ninth surface area, and implanting, into the drain region of the LDMOS transistor, an eleventh impurity region (1706) with a tenth volume having a tenth surface area, the tenth impurity region and the eleventh impurity region being of the first type.

15. The method of claim 1, further comprising:

forming a field oxide (2702) on the drain region of the LDMOS transistor.

16. The method of claim 1, wherein the conventional CMOS transistor is a conventional PMOS transistor and wherein:

the second impurity region (106) is of the first type; and

the seventh and eighth impurity regions are of the opposite second type.

17. The method of claim 1, wherein the conventional CMOS transistor is a conventional NMOS transistor and wherein:

the second impurity region (122) is of the opposite second type; and

the seventh and eighth impurity regions are of the first type.

18. A method of fabricating an LDMOS transistor and a conventional CMOS transistor together on a substrate, the method comprising:

implanting, into a source region of the LDMOS transistor, a P-body;

forming a gate oxide for the conventional CMOS transistor after implanting the P-body into the source region of the LDMOS transistor,

wherein a fixed thermal cycle associated with forming the gate oxide of the conventional CMOS transistor is not substantially affected by the implanting of the P-body into the source region of the LDMOS transistor.

19. The method of claim 18, wherein the conventional CMOS transistor is a conventional PMOS transistor or a conventional NMOS transistor.

20. The method of claim 18, wherein implanting the P-body for the LDMOS transistor includes implanting the P-body using a first implant (802) and a second implant (804).

21. The method of claim 20, wherein the first implant is a high energy implant.

22. The method of claim 20, wherein the first implant is a large angle tilt implant.

23. A method of fabricating an LDMOS transistor and a conventional CMOS transistor together on a substrate, the method comprising:

forming a gate for the LDMOS transistor, including forming an LDMOS gate oxide and covering the LDMOS gate oxide with a conductive material;

implanting, into a source region of the LDMOS transistor, a P-body, the P-body being self aligned with respect to the gate of the LDMOS transistor; and

forming a gate for the conventional CMOS transistor, including forming a gate oxide of the conventional CMOS transistor and covering the gate oxide of the conventional CMOS transistor with a conductive material,

wherein the gate of the conventional CMOS transistor is formed distinct from the gate of the LDMOS transistor.

24. The method of claim 23, wherein a thickness of the LDMOS gate oxide is similar to a thickness of the gate oxide of the conventional CMOS transistor.

25. The method of claim 23, wherein a thickness of the LDMOS gate oxide is greater than a thickness of the gate oxide of the conventional CMOS transistor

26. The method of claim 23, wherein the conventional CMOS transistor is a conventional PMOS transistor or a conventional NMOS transistor.